REMARKS

In the Final Office Action, Claims 7-8 and 22-30 are rejected and Claims 9-11 are objected to. In this Response, Claims 22 and 26 are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 7-18 and 22-30, in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

Applicants respectfully assert that the Patent Office failed to adequately set forth a *prima facie* rejections under 35 U.S.C. §§102(a), (e) or (f). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

The Examiner rejected Claims 7-8, 12-18, and 22-29 under 35 U.S.C. §§102(a), (e) and (f) as being clearly anticipated by U.S. Patent No. 6,170,052 issued to Morrison ("Morrison"). Applicants respectfully traverse these rejections.

Regarding Claim 7, Claim 7 includes the following claim features, which are neither taught nor suggested by either Morrison or the references of record:

> performing both a first operation from the first branch instruction path to produce a first result and a second operation from the second branch instruction path to produce a second result,
>
> associating both the first result and the second result with a condition associated with the identified conditional branch instruction,
>
> outputting both the first result and the second result with the associated condition, and
>
> retiring the first result or the second result based on how the condition is resolved. (Emphasis added.)

Conversely, as illustrated with reference to FIGS. 3 and 4 of Morrison, Morrison describes a renaming technique for a class of special predicated sequences 30 to form renamed predicate sequences 36 to prohibit prior art renaming:

> . . . changes the results from a predicated sequence and will produce incorrect results. (col. 2, lines 66-67.)

Accordingly, Morrison describes a class of special predicated sequences, as illustrated in FIG. 3:

> The special predicated sequence 30 also includes first and second conditional micro-ops 32, 33. The conditional micro-ops 32, 33 are executed when the condition is true and false, respectively. The first and second conditional micro-ops 32, 33 have the same logical destination register. The second conditional micro-op 33 restores the data previously stored in the register Z back in the same

> register Z when the predicate is false. Thus, the special predicated sequence 30 updates the contents of the register Z for both values, i.e. true or false of the predicate P_X. (*See* col. 4, lines 27-36.) (Emphasis added.)

According to the above-cited passage, Applicants respectfully submit that Morrison teaches the execution the first conditional micro-op 32 only condition P_X is true. Conversely, the second conditional micro-op 33 is only executed if condition P_X is false.

Although the Examiner cites block 80 of FIG. 6 of Morrison in order to illustrate a teaching that both the first and second micro-operations are executed, Applicants respectfully disagree with the Examiner's contention. In fact, Applicants respectfully submit that col. 6, lines 1-4 of Morrison contradicts the cited passage above. Furthermore, Applicants would direct the Examiner's attention to col. 8, lines 37-42 of Morrison, wherein it is stated:

> . . . the first type of predicated sequence being a sequence of micro-ops that consist of a predicated evaluating micro-op, a third micro-op, and a fourth micro-op, the third micro-op being executed in response to the predicate being true, and the fourth micro-op being executed in response to the predicate being false, the fourth micro-op being for restoring a data word to a register that previously stored the data word. (Emphasis added.)

As illustrated with reference to FIG. 4 of Morrison, execution of both conditional micro-op 38 and conditional micro-op 39 would result in overriding of the value generated by conditional micro-op 38 once conditional micro-op 39 is executed. In other words, conditional micro-op 39 restores data previously stored in the register Z_1 back into register Z_1 when P_X is false. Hence, execution of both conditional micro-op 38 and conditional micro-op 39 would only produce correct results if P_X is false. However, if P_X is true, execution of conditional micro-op 39 would restore the initial value of register Z_1, thereby overwriting the value stored in register Z_1 by execution of condition micro-op 39.

Hence, Applicants respectfully submit that Morrison fails to teach or suggest performing of both the first micro-operation from a first branch instruction path to produce a first result and a second operation from a second branch instruction path to produce a second result, as required by Claim 7. Moreover, Morrison is devoid of any teachings with reference to retiring the first result or the second result based on how the condition is resolved, as required by Claim 7. In addition, Morrison is devoid of any teachings or suggestions regarding first and second branch instruction paths, as required by Claim 7.

However, the case law is quite clear in requiring that each and every element of the claim must be exactly disclosed in the anticipatory reference. *Id.* Accordingly, Applicants respectfully submit that the Examiner fails to adequately set forth a *prima facie* case of anticipation of Claim 7 since the renaming technique for the special predicated sequences, as taught by Morrison, fails to teach or suggest execution of instructions from a first branch instruction path and a second branch instruction path, as required by Claim 7.

Therefore, Applicants respectfully submit that Claim 7 is patentable over Morrison, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claim 7.

Regarding Claims 8 and 12-15, Claims 8 and 12-15 depend from Claim 7 and therefore include the patentable claim features of Claim 7, as described. Accordingly, Claims 8 and 12-15, based on their dependency from Claim 7, are also patentable over Morrison and the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claims 8 and 12-15.

Regarding Claims 9-11, Applicants would respectfully like to thank the Examiner for acknowledging the allowability of Claims 9-11 if incorporated into independent Claim 7. However, Claims 9-11 are also patentable over Morrison and the references of record based on their dependency from Claim 7. Accordingly, Applicants respectfully request that the Examiner allow Claims 9-11.

Regarding Claim 16, Claim 16 includes the following claim feature, which is neither taught nor suggested by either Morrison or the references of record:

> a retirement unit to retire either the first result or the second result based on how the condition is resolved. (Emphasis added.)

According to the Examiner:

> Applicants retire unit in Claim 16 is merely circuitry that makes sure that it is the correct predicated result which is used subsequently. Inherently, Morrison has such circuitry or his system won't work. (*See* Final Office Action mailed 02/06/04, pg. 3.)

The Federal Circuit Court of Appeals of In Re Rijckaert, 9, F.3d 1531 (Fed. Cir. 1993) held that:

> [T]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. (9 F.3d at 1534, 28 U.S.P.Q. 2d at 1955, 1957.)

According to the Examiner, Morrison inherently includes a retirement unit, as required by Claim 16, "otherwise the system won't work". (*See Id.*) However, as indicated above with reference to Claim 7, the first and second conditional micro-operations of the special predicated sequence, as taught by Morrison, are not both executed, as required by Claim 16. Namely:

> the second conditional micro-op 33 restores a data previously stored in the register Z back in the same register Z when the predicate is false. Thus, the special predicated sequence 30 updates the contents of the register Z for both values, i.e. true or false of the predicate P_X. (col. 4, lines 32-36.)

Based on the above-cited passage, either the first conditional micro-op is executed, such that the predicate P_x is true, or the second conditional micro-op is executed, such that the P_x is false. Otherwise, execution of both the first conditional micro-operation and the second conditional micro-operation would result in incorrect results if P_x were true ; namely, the second

conditional micro-operation would restore the register Z_1 according to the contents of register Z_2, thereby overriding the value stored within Z_1 by micro-op 38. (*See* FIG. 4.)

Furthermore, Applicants respectfully submit that those skilled in the art recognize that a conventional retirement unit is designed to retire instructions, or micro-operations, once micro-operations from which the respective micro-operation depends are successfully executed. In other words, conventional retirement units do not make retirement decisions to retire either a first result or a second result based on how a condition associated with the results is resolved, as required by Claim 16.

Moreover, Applicants submit that assuming, *arguendo*, that Morrison inherently included a retirement unit, such retirement unit would not include functionality to retire either a first result of a first operation from a first instruction path or a second result from a second operation from a second instruction path based on how a condition associated with the results is resolved, as required by Claim 16.

Applicant respectfully submits that the Examiner cannot establish a *prima facie* case of anticipation since the Examiner has failed to provide a basis in fact under technical reasoning to reasonably support the determination that the alleged inherent characteristic necessarily flows from the teachings of the prior art. *Ex Parte* Levy, 17 U.S.P.Q. 2d 1461, 1464 (Bd. Pat. App. and Intr. 1990).

Consequently, Applicants respectfully submit that the Examiner has failed to establish the inherency of a retirement unit, as required by Claim 16. Hence, a *prima facie* case of anticipation of Claim 16 by Morrison has not been established. Accordingly, Claim 16 is patentable over Morrison, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claim 16.

Regarding Claims 17 and 18, Claims 17 and 18 depend from Claim 16 and therefore include the patentable claim features of Claim 16, as described above. Accordingly, Claims 17 and 18, based on their dependency from Claim 16, are also patentable over Morrison, as well as references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claims 17 and 18.

Regarding Claim 22, Claim 22, as amended, includes the following patentable claim features, which are neither taught nor suggested by either Morrison or the references of record:

> . . . an execution unit to perform both a first operation from a first instruction path designated by a conditional instruction to produce a first result and a second operation from a second instruction path designated by the conditional instruction to produce a second result and to associate both the first result and the second result with a condition associated with the conditional instruction;
>
> (b) a reorder buffer to store results of executed instructions; and

(c) a retire unit to retire results of executed instructions, the retire unit to retire the first result or the second result based on how the condition is resolved. (Emphasis added.)

As indicated above with reference to FIG. 7, Morrison fails to teach execution of both a first operation for a first instruction path and a second operation from a second instruction path, as required by Claim 16. As indicated above, Morrison teaches away from execution of first and second instructions from respective first and second branch instruction paths since such execution would result in the overriding of data stored within a register by the first conditional instruction when a predicate value evaluates to true.

Furthermore, as described above with reference to Claim 16, Morrison fails to teach or suggest a retirement unit to retire the first result or the second result based on how a condition is resolved, as required by Claim 22. Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation of Claim 22 since Morrison fails to teach or suggest each of the claim features of Claim 22, as amended. Accordingly, Claim 22 is patentable over Morrison, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claim 22.

Regarding Claims 23-25, Claims 23-25 depend from Claim 22 and therefore include the patentable claim features of Claim 22, as described above. Accordingly, Claims 23-25. based on their dependency from Claim 22, are also patentable over Morrison, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claims 23-25.

II. Rejection Under 35 U.S.C. §103

The Examiner rejected Claims 26 and 30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,430,641 issued to Kates ("Kates") in view of Carter et al. ('Carter") (*Predicated Static Single Assignment*). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 26, Claim 26, as amended, includes the following claim features, which are neither taught nor suggested by either Kates, Carter or the references of record:

a processor to perform both a first operation from a first instruction path designated by a conditional instruction to produce a first result and a second operation from a second instruction path designated by the conditional instruction to produce a second result, to associate both the first result and the second result with a condition associated with the conditional instruction, to output both the first result

and the second result with the associated condition and to retire the first result or the second result based on how the condition is resolved. (Emphasis added.)

As correctly pointed out by the Examiner, Kates provides no teachings or suggestions with reference to the above-described features of Claim 26. Accordingly, the Examiner cites Carter, which according to the Examiner, teaches the above features of Claim 26. Applicants respectfully disagree with the Examiner's contention.

As described at pg. 2 of Carter, Carter teaches a process of replacing branches with compare operations and associating operations with a predicate defined by that compare referred to as "if conversion". (*See* pg. 2, ¶1 of Carter.) As further described, Carter teaches the notion of a hyperblock:

> A hyperblock is a predicated region of code consisting of a group of basic blocks with one entry point and possibly multiple branches. As described, branches with both targets in the hyper-block are eliminated and converted to predicate definitions using if conversions. All remaining branches have targets outside the hyper block. (pg. 2, ¶2 of Carter.)

In other words, as indicated by the above-cited passage, Carter teaches the elimination of branches with both targets in the hyperblock, while all other branches remain unmodified. Conversely, Claim 26, as amended, requires the execution of a first operation from a first instruction path designated by a conditional instruction to produce a first result and execution of a second operation from a second instruction path designated by the conditional instruction to produce a second result.

In other words, Claim 26, as amended, requires executing at least first and second operations from corresponding first and second instruction paths indicated by the conditional instruction. Hence, Claim 26 does not replace branches with conditional instructions, but performs the operations associated with instruction paths designated by the conditional instruction and simply retires those instructions which were on the path designated by evaluation of a conditional instruction associated with the first and second results.

Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 26 over Kates in view of Carter since the combination of the references fails to teach or suggest each of the claim features of Claim 26, as described above.

Furthermore, Applicants respectfully submit that the Examiner fails to show a teaching or suggestion to combine the teachings or modify the teachings of Kates in view of Carter. Namely, the Examiner fails to allude to any teaching or suggestion within Kates regarding predicated execution of branch instructions or out-of-order execution. Specifically, Applicants submit that one skilled in the art would not modify Kates, as proposed by the Examiner, since the skill in the art would provide no suggestion or teaching for the proposed combination.

Accordingly, Applicants respectfully submit that the features of Claim 26 could only be arrived at through inappropriate hindsight. However, it is well established that obviousness cannot

be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospital Sys., Inc. v. Montefiore Hospital, 732 F.2d. 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Also, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967).

Therefore, Applicants respectfully submit that a *prima facie* case of obviousness of Claim 26 over Kates in view of Carter, due to the fact that the Examiner fails to illustrate a teaching or suggestion to combine the reference teachings. Accordingly, Claims 26, as amended, is patentable over Kates, Carter and the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claim 26.

Regarding Claims 27-30, Claims 27-30 depend from Claim 26 and therefore include the patentable claim features of Claim 26, as described above. Accordingly, Claims 27-30, based on their dependency from Claim 26, are also patentable over Kates, Carter and the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and allow Claims 27-30.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: April 30, 2004

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 30, 2004

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Marilyn Bass April 30, 2004